FT-UNSHADES2: A Platform for early evaluation of ASIC and FPGA dependability using partial reconfiguration

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Abstract—**Fault injection is a widely accepted method for the evaluation of device and system reliability, by mean of dynamic analysis of a digital circuit implemented in a FPGA. A set of test vectors is applied and output vectors are monitored while a number of faults are injected deliberately. The fault injection strategy in our platform consists of a controlled modification of the FPGA's configuration memory affecting the targeted netlist nodes. The output data sequence is checked cycle by cycle to detect any upset in it. In the new FTUNSHADES2 platform, the partial reconfiguration capability featured in Xilinx FPGAs is exploited to speed-up the full process of fault injection. The platform is not only designed for fault injection in a traditional way, but also to evaluate the dependability on digital designs intended to run on FPGAs and as a testbed for beam experiments on different devices. We are introducing an original architecture with a software interface able to manage all the operation modes, improving the capabilities of the existing platforms.**

Keywords—**Single Event Effect, Partial Reconfiguration, Prototyping Platform, Fault Tolerance.**

I. INTRODUCTION

THe use of configurable devices (FPGA) for the evaluation of reliability of integrated circuits is not a novelty[1]. The concept of Rapid Prototyping is closely related to reconfigurable devices and standard design guidelines for integrated circuits always recommend the implementation of new designs in such emulation and debugging devices. One of the most relevant properties in a digital design that can be evaluated by fault injection techniques is the reliability. Fault injection involving different fault models has been object of study from long ago [2].

There is a range of different techniques for different fault models. Circuit implementation in a configurable device together with fault modeling allows one to perform high-speed fault analysis and an accurate evaluation of the dynamic behavior of the circuit under test (CUT). Certainly, all these hardware based techniques are reproducible by software simulation, even allowing for more detailed analysis with respect to some emulation platforms.

Particularly, one of the most interesting applications demanded currently is the Single Event Effects (SEE) analyzers. The term SEE makes reference to the capability of ionizing radiation to disrupt the operation of integrated circuits. Ionizing radiation passing through a semiconductor generates a track of charge that under some circumstances, can be collected by a circuital node provoking a voltage transient and even a bit-flip in a register or memory cell. As technology scales down, the occurrence of these phenomena is becoming more and more frequent and therefore it is raising big concerns [3]. Traditionally, radiation hardness assurance was a requirement for devices intended to operate in space missions. In the present, there are also a number of standards and specifications related to the effects of radiation in avionics or automotive industry.

II. PLATFORMS AND METHODS FOR FAULT ANALYSIS.

The development of hardware platforms for fault injection based on FPGAs started some years ago. To the existing software solutions [4], a repertoire of different implementation strategies were put under development to take advantage of the possibilities of configurable hardware. The capability to run a design at nominal clock frequencies makes it possible to complete campaigns with a huge number of fault injections, covering all the configuration space (registers x no. of cycles) in a reasonable period of time [5]. In most cases, the computation time would be prohibitive for software fault injection platforms.

The usage of hardware platforms is oriented to fault injection tests, generally bit-flips (this term is explained in detail in section III), on digital circuits running on a FPGA. There are several approaches to inject faults. A common methodology consists of embedding extra circuitry in the original design to externally force logical faults. The main advantage is the generality of the method. This extra circuitry is called *instrument* and the whole circuit is said to be *instrumented*.

In addition to the use of circuit prototyping in FPGAs, in the case of Xilinx devices, it is also available a way to inject faults using the configuration resources. The main advantage of this approach is the simplicity of use, as far as only a netlist synthesis targeting a Xilinx FPGA is needed. The injection mechanism is inherent to Xilinx FPGAs internal circuitry. Therefore, only FPGAs from this vendor are available for this procedure. There is also a timing consideration since a timeout is required in the dynamics of the system to proceed with the fault injection. Nevertheless, it is possible to develop a variety of analysis processes associated to these concepts.

The reconfiguration mechanism deployed in the Xilinx FPGAs and usable for fault injection purposes is known as *Capture & Readback*, that essentially consists of a bitmap with register locations that can be easily modified. For this task, we have exploited the available SelectMap parallel configuration port.

III. SINGLE EVENT EFFECTS: MODELING AND EVALUATION

Single Event Effects (SEE) are originated after high-energy ionizing particles strike a semiconductor nearby a sensible node in a digital circuit, producing in some cases unwanted changes depending on the state of the registers, i.e. the status of the whole system. These events are termed “single” since they are related to unique particle strikes. Attending to the effects in the circuit can be classified as:

- Single Event Upset (SEU) when only a register is affected,
- Single Event Transient (SET) when the voltage perturbation after the strike affects combinational logic and propagates to the circuit registers where is sampled, or
- Multi Bit Upset (MBU) when several registers are affected simultaneously.

The simplest fault model for an event is the bit-flip.

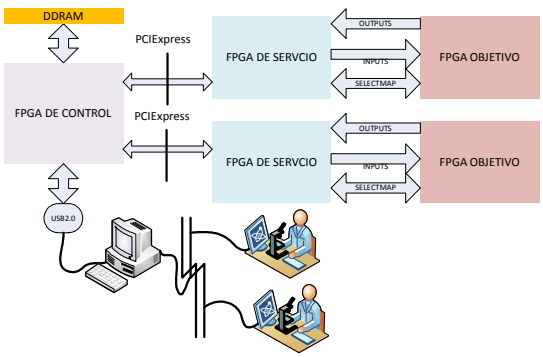

Fig. 1. Basic scheme of the system FT-UNSHADES2 showing interconnection

The classic conception of a typical system for evaluation of circuit reliability against SEE is made up of two FPGA platforms running synchronously stimulated with the same set of test vectors, with their outputs being compared cycle by cycle. One of the testing platforms (faulty) hosts the circuit and the fault injection mechanism, the other one (gold) hosts only the circuit running fault-free. This setup allows powerful analysis capabilities, since it is possible to inspect the internal state and compare the corresponding values for each register.

In FT-UNSHADES2 the bit-flip is performed by changing the logic value of internal registers using the allocation file provided by standard Xilinx tools during the implementation workflow. It is done by partial reconfiguration. With precise control of the system clock, the exact clock cycle for bit-flip is determined. Finally, the user decides the number of simultaneous fault injections and their correlation, to emulate MBUs or SETs.

The platform allows one to work in an FPGA evaluation mode, i.e. testing the reliability of the device while configured with a given digital design. The vulnerabilities in this case are the configuration bits in the SRAM-FPGA deployed in the current emulation platform. The test system has been designed for these purposes, making it necessary a previous static evaluation of the criticality of the configuration bits [6].

IV. NEW ARCHITECTURE

The architecture of the new platform inherits much of the technology developed for the previous platform FT-UNSHADES [7,8,9]. It is conceived as a hardware platform managing communications with a Host PC running a powerful human-machine interface named TNT3, as seen in Fig. 1. Through a USB-link, the platform receives the Target-FPGA configuration, the set of stimuli and the injection points.

For the sake of higher flexibility, we have introduced three main hardware blocks in the architecture; a motherboard (Fig. 2) and two daughterboards (Fig. 3), plugged into a pair of PCIExpress slots. The current motherboard is a standard Xilinx ML510 board with a Virtex-5 XC5VFX130T which is known as the Control FPGA. The serialization via the PCIE link makes the system independent on the number of inputs/outputs of the design under test, with a max number of I/Os of 512. The daughterboards are full-custom designs in FT-UNSHADES2. Each daughterboard features two FPGAs with one of them being a Virtex-5 including an embedded PPC450. This is called the Service-FPGA, and is used to interface communications with the motherboard and to manage a number of operations like applying input stimuli,

reading outputs, configuration of the Target-FPGA and for fault injection tasks. The FPGA to be injected is of free choice (the daughterboard must be adapted to fit a different FPGA), in our first prototype we chose a Virtex-5. This Target-FPGA implements the design under test and is completely controlled by the Service-FPGA. The SelectMAP port on the Target-FPGA is accessed by the Service-FPGA to manage all the configuration tasks. The Target-FPGA device should be elected attending to its capacity and connectivity to Service-FPGA.

The connection diagram showed in Fig. 1 represents the basic schema of the platform, with all the main tasks involved within each block. The application running in the Host PC (TNT3) commands all the operations required to accomplish a complete fault injection campaign like applying input stimuli, performing configuration, fault injection and status readouts.

The task distribution for the different blocks is as follows:

- HostPC. Is the human-machine interface. It generates and sends the configuration files to the hardware platform. Defines the injection models and selects the testbenches. Interacts *step-by-step* with the platform in the analysis mode.
- Control-FPGA. Interfaces the DDR modules in the motherboard: saves the Target-FPGA configuration bits, the set of stimuli and the fault list, it additionally stores the results of the outputs comparison. Moreover, it manages the operation commands and the PCIExpress links.
- Service-FPGA. It interacts with the Control-FPGA through the PCIExpress link. It codes the stimuli and decodes the outputs from the DUT (Device Under Test). It also performs configuration tasks and fault injection in the Target-FPGA.

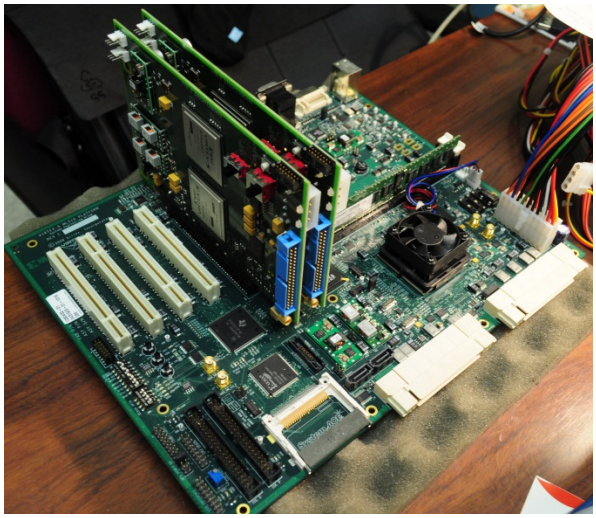

Fig 2. Picture of the complete platform. The Control-FPGA is on the ML510 motherboard and the other FPGAs on the other two daughterboards.

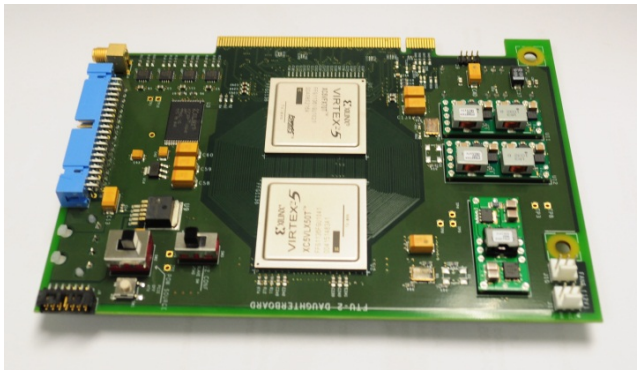

Fig 3. Picture of a full-custom daughterboard. Close to the PCIExpress card-edge (upside) is the Service-FPGA and below it is the Target-FPGA.

V. SPECIFIC FEATURES

The operation modes developed in FT-UNSHADES2 provide the following capabilities:

1. Fault injection in campaign mode over the RTL description of a digital design, as done commonly, featuring fault models for SEU, SET and MBU events. In this mode of operation, one of the two daughterboards performs as the injector and the other one as the error-free reference. The outputs from both boards can be checked synchronously to find *errors*, or register to register, to detect *latent* faults or even detect *silent* faults (faults overwritten or filtered). This operation mode supports a “single-step” analysis, i.e. to execute a testbench cycle by cycle comparing all the registers in the design with the error-free replica. This kind of tests provide a detailed analysis on the propagation of faults through the structure of registers, becoming a RTL-simulator.

2. Fault injection in the configuration bits. Considering the FPGA as the final target device, i.e. the effects of radiation on the design are evaluated by the damage induced in the SRAM FPGA configuration. This mode requires a previous analysis of criticality for the configuration bits to identify harmless fault injection, reducing considerably the fault injection campaign. This analysis is closely related to the FPGA technology and depends on the design implemented. There are tools like *Star-Rora* [10] from the Politecnico di Torino that provide a subset of points to inject that are potentially sensitive. One of the main advantages of the platform is that it is possible to redesign only part of the daughterboard to replace the FPGA device by another part of interest. By now, we have available several parts from the Virtex-5 family.

3. Beam test mode is achieved by replacing the Target-FPGA by an ASIC to get a complete testbed

for radiation experiments. This operation mode is suitable for tests in particle accelerators or laser beam facilities. There is always an error-free reference design running in one of the daughterboards for comparison. The advantage of this schema is that while the ASIC is under radiation, a replica of the design is running in an FPGA with all the content of the design immediately accessible.

VI. USER TOOLBOX

One of the main contributions of the new platform is the user interface. The workflow for design preparation is significantly simplified because now only a valid User Constraint File (UCF) is required complying with the Target-to-Service FPGA hardware interconnection. The set of stimuli is obtained directly from VHDL simulation in a standard simulator. So that, test preparation is straightforward and takes no much time.

The user interface was conceived as a remote assistant to minimize data transactions between the user and the platform. A server can support several platforms connected and so the system selects the one available. Furthermore, the web server allows remote access and full operability just using a client web browser (see Fig. 4). The interface is user friendly, with drop-down menus that make it easy to take advantage of all the features of the system.

The tool provides procedures for detailed analysis, as the mentioned single-step analysis, including the generation of waveforms. In addition, the tool provides a set of algorithms for exhaustive analysis of the data extracted during operation. Among these are the hierarchical criticality analysis and the detection of critical faults (see Fig. 5 and 6). Finally, a complete testing language has been developed to define the fault injection model and the characteristics of the campaign.

Fig 4. Login page of the system FT-UNSHADES2.

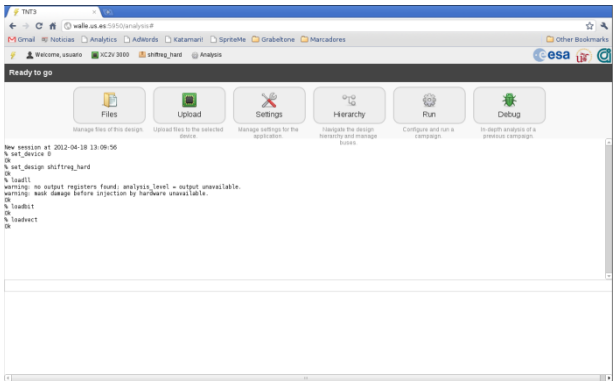

Fig 5. Screenshot showing the toolbox of FT-UNSHADES2.

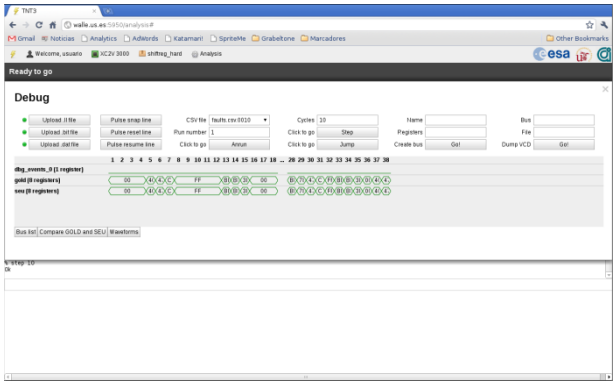

Fig 6. Screenshot showing FT-UNSHADES2 working in detailed analysis mode.

VII. SYSTEM CAPABILITIES

The system has been characterized to find out bottlenecks in the process of injection. For the adopted architecture, the speed limit is in the serial data transfer of the PCIExpress link. In the previous FT-UNSHADES platform, the fault injection rate was near 100 faults per second.

First estimations for maximum DUT clock frequencies are around 100 MHz, but it depends on the number of inputs and outputs. A fault rate of roughly 10,000 faults per second can be achieved in designs with 32 inputs and outputs or less, deploying only one lane of the PCIExpress link (PCIE x1).

In the former FT-UNSHADES platform, the continuous USB transactions were the bottleneck, now many operations are embedded in hardware and data transfer to the host PC has been minimized. In the newer FT-UNSHADES2, the component limiting speed (in some cases) is the PCIExpress, but the link can be expanded to 8 lanes for high-throughput performance.

VIII. CONCLUSIONS

FTU2 is a hardware-based fault injection prototype that could be one of the most powerful tools for Single Event Effects evaluation of new deep sub-micron digital designs. The flexibility and resources available make FTU2 appropriate for different uses, not just as a hardware emulator for fault injection techniques but a customizable tool for other uses such as ion beam

experiments, acting as a coincidence detector [11]. A number of major improvements have been introduced with respect to the former FT-UNSHADES system. The new platform offers complete flexibility and high fault injection rates, conserving a detailed step-by-step mode of analysis. More complex designs can be tested with the only requirement that the design must fit in a single Xilinx FPGA. Finally, remote access makes it easier for the final user to accomplish fault injection campaigns.

ACKNOWLEDGEMENTS

The present work has been funded by the project CICYT TEC2010-22095-C03-01 of the Ministry of Economy and Competitiveness of Spain. In addition, the project FT-UNSHADES is funded by the RTP program from the European Space Agency (ESA)

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